COPY

Dkt. 2271/71388

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentees: Junji ICHIMIYA

Patent No.: 7,076,756 Serial No.: 10/701,249

Issued: July 11, 2006 Filed: November 4, 2003

For: LAYOUT DESIGN METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT, WITH HIGH INTEGRATION LEVEL OF MULTILEVEL METALLIZATION

I hereby certify that this correspondence is being deposited this date with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Paul Teng June 27, 2007
Paul Teng Date
Reg. No. 40,837

1185 Avenue of the Americas
New York, N.Y. 10036
(212) 278-0400

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN.: Certificate of Correction Branch

SIR:

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. §1.322

Please find a Patent Office form PTO-1050, attached hereto as **Exhibit A**, indicating errors in the above-identified patent.

The errors being corrected on form PTO-1050 are as follows.

The Title of the patent should read as follows:

LAYOUT DESIGN METHOD ~~OF~~ FOR SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT, WITH HIGH INTEGRATION LEVEL OF ~~MULTIPLE-LEVEL~~ MULTILEVEL METALLIZATION

Patentee respectfully requests that the Patent Office issue a Certificate of Correction under 37 C.F.R. §1.322 which provides

for the correction of "a mistake in a patent, incurred through the fault of the Office, which mistake is clearly disclosed in the records of the Office."

Patentee maintains that the above-mentioned mistakes are clearly disclosed in the records of the Patent and Trademark Office.

The correct Title is clearly reflected in the file history of Serial No. 10/701,249, from which the subject patent issued. The title was amended in Serial No. 10/701,249 by an Amendment filed December 1, 2005. A copy of the December 1, 2005 Amendment and a photocopy of the postcard returned by the Patent Office which includes a stamp indicating that the Patent Office received the December 1, 2005 Amendment are attached hereto as **Exhibit B.**

The amended title of Serial No. 10/701,249 was approved via a February 27, 2006 Notice of Allowance and Notice of Allowability. A copy of the February 27, 2006 Notice of Allowance and Notice of Allowability is attached hereto as **Exhibit C.** The February 27, 2006 Notice of Allowability indicates that the amendment to the title was approved.

In addition, applicant indicated, when paying the issue fee, that the Title of the patent should be the amended title. A copy of the Fee(s) Transmittal submitted along with the issue fee and publication fee on May 24, 2006 is attached as Exhibit D hereto.

Therefore, Patentee maintains that the errors appearing in

the Title of the subject patent were mistakes incurred through the fault of the Patent Office and is clearly disclosed in the records of the Patent Office.

Accordingly, Patentee respectfully requests that a Certificate of Correction be issued by the Patent Office.

No fee is deemed necessary in connection with the filing of this Request for a Certificate of Correction under 37 C.F.R. §1.322. However, if any additional fee is deemed necessary, authorization is hereby given to charge the amount of such fee to Deposit Account No. 03-3125.

If a Petition is required to effect correction of the above-mentioned mistakes in the patent, please deem this Request to be such a Petition, and charge any fees deemed necessary for such Petition, to Deposit Account No. 03-3125.

Respectfully submitted,

PAUL TENG, Reg. No. 40,837
Attorney for Patentees
Cooper & Dunham LLP
Tel.: (212) 278-0400

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,076,756

APPLICATION NO : 10/701,249

ISSUE DATE : July 11, 2006

INVENTOR(S) : Junji ICHIMIYA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Replace the Title section on the cover page of the patent, with the following:

--(54) LAYOUT DESIGN METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT, WITH HIGH INTEGRATION LEVEL OF MULTILEVEL METALLIZATION--

MAILING ADDRESS OF SENDER:

Cooper & Dunham LLP
1185 Avenue of the Americas
New York, New York 10036

Applicant: **Junji ICHIMIYA, S.N. 10/701,249**

Client: **RICOH (2271)** File No. **71388** Atty. **ISK/PT**

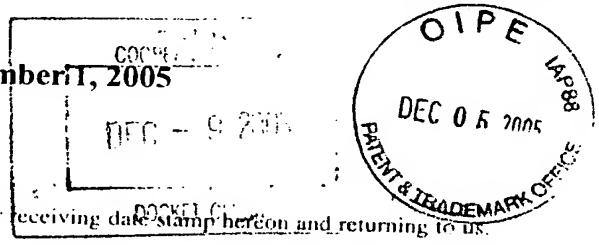
Date: **December 1, 2005**

Kindly acknowledge receipt of the accompanying

In connection with Serial No. 10/701,249:

1. Amendment, including Certificate of Mailing dated December 1, 2005.

DUE DATE: December 1, 2005



by placing your receiving date stamp hereon and returning to us.

JUL 3 2007

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed when appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address a indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" fo maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 02/27/2006

Ivan S. Kavrukov, Esq.
Cooper & Dunham LLP
1185 Avenue of the Americas
New York, NY 10036

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Paul Teng (Depositor's name)
Paul Teng 5/24/2006 (Signature)
May 24, 2006 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,249	11/04/2003	Junji Ichimiya	2271/71388	6111

TITLE OF INVENTION: LAYOUT DESIGN METHOD ~~OF~~ FOR SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT, WITH HIGH INTEGRATION LEVEL OF ~~MULTIPLE LEVEL METALIZATION~~ MULTI-LEVEL METALLIZATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	05/30/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
TO, TUYEN P	2825	716-010000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 COOPER & DUNHAM LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Ricoh Company, Ltd.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Tokyo, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 3

4b. Payment of Fee(s):
☒ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 03-3125 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Paul Teng Date May 24, 2006
Typed or printed name Paul Teng Registration No. 40,837

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Dkt. 2271/71388

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Junji ICHIMIYA

Serial No.: 10/701,249 Group Art Unit: 2825

Date Filed: November 4, 2003 Examiner: Tuyen To

For: LAYOUT DESIGN METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT

I hereby certify that this correspondence is being deposited this date with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Paul Teng December 1, 2005
Paul Teng Date
Reg. No. 40,837

1185 Avenue of the Americas
New York, N.Y. 10036
(212) 278-0400

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

This Amendment is submitted in response to the Office Action dated September 8, 2005 in connection with the above-identified application.

Amendment to the Title begins on page 2 of this paper.

Amendments to the Claims are reflected in the **Listing of Claims** section which begins on page 3.

Remarks begin on page 7 of this paper.

JUL 3 2007

JUL 3 2007

Amendment to the Title

Please amend the Title to the following:

--LAYOUT DESIGN METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT, WITH HIGH INTEGRATION LEVEL OF MULTILEVEL METALLIZATION--.

Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (original) A layout design method for a semiconductor integrated circuit, comprising the steps of:

providing a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells, each filler cell acting to fill space between the functional cells, one of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal, and another of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail one of which is connected to the upper-layer metal through a via;

arranging the functional cells on a layout based on the structural information from the layout library; and

arranging the filler cells of any of the plurality of groups selectively based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells are not located on the layout, each channel region being located at a predetermined distance from signal lines on the layout.

2. (original) The layout design method of claim 1 wherein the filler cells of at least one of the plurality of groups are arranged in the channel regions where standard cells and macro cells are not located on the layout, and power supply lines are arranged on the layout so that the filler cells of said at least one group are connected to the power supply lines.

3. (original) The layout design method of claim 1 wherein the filler cells of at least one of the plurality of groups which contain a bypass capacitor are arranged on the layout.

4. (original) The layout design method of claim 1 wherein the filler cells of at least two of the plurality of groups have a common configuration with respect to intermediate layers between an uppermost layer and a lowermost layer of the layout.

5. (original) The layout design method of claim 1 wherein the filler cells are selectively arranged in the channel regions on the layout so that metal layers of the filler cells which are not connected to the signal lines are connected to power supply lines on the layout.

6. (original) The layout design method of claim 1 wherein a duplicate arrangement of the filler cells of at least one of the plurality of groups is provided over a standard-cell region or a macro-cell region of the layout.

7. (original) A semiconductor integrated circuit which is created by a layout design method using a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells, each filler cell acting to fill space between the functional cells, one of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal, and another of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail one of which is connected to the upper-layer metal through a via, the semiconductor

integrated circuit comprising:

the functional cells arranged on a layout based on the structural information from the layout library;

signal lines arranged on the layout; and

the filler cells of any of the plurality of groups selectively arranged based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells are not located on the layout, each channel region being located at a predetermined distance from the signal lines on the layout.

8. (original) The semiconductor integrated circuit of claim 7 wherein the filler cells of at least one of the plurality of groups are arranged in the channel regions where standard cells and macro cells are not located on the layout, and power supply lines are arranged on the layout so that the filler cells of said at least one group are connected to the power supply lines.

9. (original) The semiconductor integrated circuit of claim 7 wherein the filler cells of at least one of the plurality of groups which contain a bypass capacitor are arranged on the layout.

10. (original) The semiconductor integrated circuit of claim 7 wherein the filler cells of at least two of the plurality of groups have a common configuration with respect to intermediate layers between an uppermost layer and a lowermost layer of the layout.

11. (original) The semiconductor integrated circuit of claim 7 wherein the filler cells are selectively arranged in the channel regions on the layout so that metal layers of the filler cells which are not connected to the signal lines are connected to power supply lines on the layout.

12. (original) The semiconductor integrated circuit of claim 7 wherein a duplicate arrangement of the filler cells of at least one of the plurality of groups is provided over a standard-cell region or a macro-cell region of the layout. .

13. (new) The layout design method of claim 1 wherein the arrangement of the filler cells in the channel regions connects power supply wiring of the upper layer metal and power supply wiring of the lower-layer metal.

14. (new) The layout design method of claim 13 wherein the arrangement of the filler cells in the channel regions connects said upper layer metal to one of said power rail and said ground rail of said lower-layer metal.

15. (new) The layout design method of claim 1 wherein the filler cells are arranged in the channel regions after wiring of signal lines is performed.

REMARKS

The application has been reviewed in light of the Office Action dated September 8, 2005. Claims 1-12 were pending. By this Amendment, new dependent claims 13-15 have been added. Accordingly, claims 1-15 are now pending, with claims 1 and 7 being in independent form.

The title was objected to as purportedly not sufficiently descriptive.

By this Amendment, the title has been amended to be more descriptive of the application.

Claims 1-12 were rejected under 35 U.S.C. §102(e) as purportedly anticipated by U.S. Patent No. 6,618,847 to Hulse et al.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1 and 7 are patentable over the cited art, for at least the following reasons.

This application relates to a layout design method for a multi-layered semiconductor integrated circuit. Applicant devised improved layout design techniques for a multi-layered semiconductor integrated circuit having multilevel metallization whereby power supply wiring does not need to be completely performed on the layout before wiring of signal lines is performed, and connection of the power supply wiring of an upper-layer metal and power supply wiring of a lower layer metal can be performed after the wiring of signal lines.

For example, independent claim 1 is directed to a layout design method for a semiconductor integrated circuit which includes providing a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells. Each filler cell acts to fill space between the functional cells. Moreover, one of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal. Another of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail, one of which is connected to the upper-

layer metal through a via. The cells are arranaged on a layout as follows: (a) the functional cells are arranged on the layout based on the structural information from the layout library; and (b) the filler cells of any of the plurality of groups are arranged selectively based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells are not located on the layout, each channel region being located at a predetermined distance from signal lines on the layout. Thus, the connection of the power supply wiring of the upper-layer metal and the power supply wiring of the lower-layer metal is made through arrangement of the filler cells after the wiring of signal lines.

Hulse, as understood by Applicant, is directed to a layout design tool which allows a user to automatically intersperse capacitor filler cells around standard cell logic (see Hulse, lines 58-65). Hulse discloses at column 5, lines 25-43 that additional tools may be used in addition to the layout design tool to route wiring, based on a a generated netlist, to each of the components, and that metal layers, wiring layers, vias, connection pads are formed based on the routing information. Hulse further discloses at column 4, lines 58-65 that each of the capacitor filler cells includes power and ground rails.

However, Hulse does not disclose or suggest performing connection of power supply wiring of an upper-layer metal and power supply wiring of a lower layer metal in a multi-layered semiconductor integrated circuit having multilevel metallization, after the wiring of signal lines, as provided by the claimed invention of the present application.

Hulse merely states that the capacitor filler cells extend the power and ground rails from adjacent standard cells, but does not disclose or suggest that the filler cells are arranged to connect power supply wiring of an upper-layer metal and power supply wiring of a lower layer metal.

Applicant does not find disclosure or suggestion in the cited art, however, of a layout design method for a semiconductor integrated circuit which includes providing a cell layout

library which stores structure information of functional cells and a plurality of groups of filler cells, wherein one of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal, and another of the plurality of groups of filler cells contains an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail, one of which is connected to the upper-layer metal through a via, as provided by the claimed invention of claim 1.

Independent claim 7 is patentably distinct from the cited art for at least similar reasons.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1 and 7, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
Tel.: (212) 278-0400

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 02/27/2006

Ivan S. Kavrukov, Esq.
Cooper & Dunham LLP
1185 Avenue of the Americas
New York, NY 10036

EXAMINER	
TO, TUYEN P	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/27/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,249	11/04/2003	Junji Ichimiya	2271/71388	6111

TITLE OF INVENTION: LAYOUT DESIGN METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT, WITH HIGH INTEGRATION LEVEL OF MULTIPLE LEVEL METALIZATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	05/30/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

3 2007

71388 1SK

Notice of Allowability	Application No.	Applicant(s)	
	10/701,249	ICHIMIYA, JUNJI	
	Examiner	Art Unit	TT
	Tuyen To	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/05/2005*.

2. ☒ The allowed claim(s) is/are *1-15*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

IssueFeeDue 5/30/06
RebiFeeDue: 5/30/06

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

A. M. Thompson
Primary Examiner
Technology Center 2800

MAY 03 2007

DETAILED ACTION

1. This is a response to the amendment and remarks/arguments filed on 12/05/2005.

2. Claims 1-15 are pending.

3. The amended title has been approved.

4. New dependent claims 13-15 have been added.

Allowable Subject Matter

5. **Claims 1-15** contain allowable subject matter.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not teach or fairly suggest a layout design method for a semiconductor integrated circuit comprising: providing a cell layout library which stores a plurality of groups of filler cells, each filler cell acting to fill space between the functional cells, one of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal, and another of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail one of which is connected to the upper-layer metal through a via; and arranging the filler cells of any of the plurality of groups selectively based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells

are not located on the layout, each channel region being located at a predetermined distance from signal lines on the layout.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. M. Thompson
Primary Examiner
Technology Center 2800

Tuyen To

Patent examiner

AU 2825